APPLICATION

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TITLE: APPARATUS FOR REDUCING A MAGNITUDE OF A RATE OF CURRENT CHANGE OF AN INTEGRATED CIRCUIT

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APPARATUS FOR REDUCING A MAGNITUDE OF A RATE OF CURRENT CHANGE OF AN INTEGRATED CIRCUIT

Background of Invention

[0001]   As technology improves, integrated circuits, such as microprocessors, continue to become faster and more powerful. However, the benefits of increased speed and higher data throughput must be balanced with the costs of increased power consumption and higher operating temperatures.

[0002]   When a microprocessor (also known in the art as a "central processing unit" or "CPU") approaches or exceeds a certain power or temperature threshold, the microprocessor must be powered down to avoid microprocessor malfunction or damage. For example, if a microprocessor's cooling system fails, the microprocessor must be shut down quickly in order to avoid overheating. Similarly, if a microprocessor is drawing power in a manner that adversely affects other computer chip components, the microprocessor must be powered down to avoid undesirable effects.

[0003]   However, the high-power nature of a microprocessor makes it difficult to power the microprocessor down instantly because doing so might cause damage to a computer chip's power supplies. The magnitude of such an instant change in current would be so high that a large change in voltage might result potentially damaging not only power supplies, but also computer chip components. Equation 1 shows the relationship between voltage, change in time, and change in current:

$$V = Z * i \qquad\qquad (1)$$

where V represents voltage, Z represents impedance, and i represents current. Thus, it follows that when i is instantly decreased, V decreases at a rate that a typical computer chip cannot sustain.

[0004]   Figure 1 shows a typical relationship (10) between current and time when power to a microprocessor, or other integrated circuit, is decreased instantly to a desired level. Particularly, Figure 1 shows the rate of current change, $\Delta i/\Delta t$, when current is reduced from 10 amps to 5 amps.

Summary of the Invention

[0005]   According to one aspect of the present invention, an apparatus for reducing a magnitude of a rate of current change of an integrated circuit comprises a control stage that generates a control signal dependent on whether power consumption by the integrated circuit needs to be reduced, and a counter stage that inputs the control signal and generates a plurality of sequential signals to a plurality of transistors, where the plurality of transistors source current from a power supply.

[0006]   According to another aspect, a circuit for reducing a rate of current change of a microprocessor comprises a control stage that is connected to a power terminal and a ground terminal, where the control stage generates a control signal, and a counter stage that inputs the control signal and a clock signal, where the counter stage generates a first signal to a gate terminal of a first transistor.

[0007]   Other aspects and advantages of the invention will be apparent from the following description and the appended claims.

Brief Description of Drawings

[0008]   Figure 1 shows a typical relationship between current and time when power is reduced.

[0009]   Figure 2a shows a diagram of a circuit in accordance with an embodiment of the present invention.

[0010]   Figure 2b shows a relationship between current and time in accordance with the embodiment shown in Figure 2a.

Detailed Description

[0011]   The present invention relates to a method and apparatus for reducing a magnitude of a rate of current change of a microprocessor or other integrated circuit. Further, the present invention relates to a method and apparatus for powering down a microprocessor or other integrated circuit. Further, the present invention relates to a method and apparatus for cooling down a microprocessor or other integrated circuit.

[0012]   Figure 2a shows a diagram of an exemplary circuit in accordance with an embodiment of the present invention. Particularly, Figure 2a shows a micro-architectural block (also referred to as "micro-architectural stage") (30) that generates a signal, **m_out**, to control a counter block (also referred to as "counter stage") (32), where the counter block (32) may include a finite state machine such as a counter (not shown). The counter block (32), which inputs a clock signal, **CLK**, for timing and counting purposes, generates signals, C_0, C_1, C_2, and C_3, to a first transistor (34), a second transistor (36), a third transistor (38), and a fourth transistor (40), respectively. When a particular transistor shown in Figure 2a is 'on,' i.e., enabled, that particular transistor behaves as a current source in that it sources current from V_{DD} (42) to V_{SS} (44). When a particular transistor is 'off,' i.e., is disabled, the current sourced through that particular transistor is decreased.

[0013]   The counter block (32) generates a low signal successively on C_0, C_1, C_2, and C_3 on positive edges of **CLK**. However, those skilled in the art will appreciate that in other embodiments, the counter block (32) may be designed differently.

[0014]   Those skilled in the art will also appreciate that in other embodiments, a different amount of signals generated by the counter block (32) may be used. Further, those skilled in the art will appreciate that in other embodiments, a different amount of transistors may be used. Further, those skilled in the art will

appreciate that the micro-architectural block (30) may be a thermal sensor that is used to power down a microprocessor when the microprocessor is about to or begins to overheat.

[0015]   Figure 2b shows a relationship (46) between current and time based on the signals and circuit shown in Figure 2a. When **m_out** is high (48), the counter block (32) generates high values on C_0, C_1, C_2, and C_3, where, in turn, the first, second, third, and last transistors (34, 36, 38, 40) are all switched 'on.' In this case, the transistors (34, 36, 38, 40) collectively source 10 amps from V_{DD} (42) to V_{SS} (44).

[0016]   When **m_out** goes low (50), the counter block (32) generates low values on C_0, C_1, C_2, and C_3 successively at positive edges on **CLK**. Thus, at the first positive edge on **CLK** after **m_out** goes low (50), the counter block (32) generates a low value on C_0 (52), which, in turn, causes the first transistor (34) to switch 'off,' effectively reducing the collective current sourced by the transistors (34, 36, 38, 40) from V_{DD} (42) to V_{SS} (44). At the next positive edge on **CLK**, the counter block (32) generates a low value on C_1 (54), which, in turn, causes the second transistor (36) to switch 'off,' effectively reducing the collective current sourced by the transistors (34, 36, 38, 40) from V_{DD} (42) to V_{SS} (44). At the next positive edge on **CLK**, the counter block (32) generates a low value on C_2 (56), which, in turn, causes the third transistor (38) to switch 'off,' effectively reducing the collective current sourced by the transistors (34, 36, 38, 40) from V_{DD} (42) to V_{SS} (44). At the next positive edge on **CLK** after **m_out** goes low (50), the counter block (32) generates a low value on C_3 (58), which, in turn, causes the last transistor (40) to switch 'off,' effectively reducing the collective current sourced by the transistors (34, 36, 38, 40) from V_{DD} (42) to V_{SS} (44).

[0017]   Those skilled in the art will appreciate that whenever a transistor is disabled, the amount of reduction of current sourced from V_{DD} (42) to V_{SS} (44) is

less than in the case where only one transistor is used to source current from V_{DD} (42) to V_{SS} (44). Thus, by gradually reducing the current sourced from V_{DD} (42) to V_{SS} (44), the magnitude of the rate of current change, or $\Delta i/\Delta t$, is less than in the case where the current reduction is effected by simply instantly reducing the current to a desired level.

[0018]   Advantages of the present invention may include one or more of the following. In some embodiments, because a plurality of transistors are used to reduce power consumption, a magnitude of a rate of current change of a microprocessor is reduced, and the microprocessor runs quieter, i.e., less noise, than when only one transistor is used to reduce power consumption.

[0019]   In some embodiments, because a magnitude of a rate of current change of a microprocessor is reduced gradually as opposed to suddenly, the microprocessor operates faster.

[0020]   In some embodiments, because a magnitude of a rate of current change of a microprocessor is reduced gradually instead of suddenly, the chance of power supply damage is reduced.

[0021]   In some embodiments, because a magnitude of a rate of current change of a microprocessor is reduced gradually as opposed to suddenly, the effect on average power consumption is reduced.

[0022]   While the invention has been described with respect to a limited number of embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be devised which do not depart from the scope of the invention as disclosed herein. Accordingly, the scope of the invention should be limited only by the attached claims.